Zero Temperature Coefficient behavior for Diamond MOSFET

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***Abstract*—The zero temperature coefficient (ZTC) is investigated by three-dimensional numerical simulations in the Diamond (hexagonal gate geometry) layout style (DSL) for Metal–Oxide–Semiconductor Field Effect Transistor, considering the same channel widths (W), gate areas (A_G) and bias condition (BC). In this work was used a simple model which predicts the ZTC point taking into account only the mobility degradation factor (c) and threshold voltage (Vth) parameters as function of temperature is proposed in the linear and saturation operation regions. The analysis takes into account the temperature variations of the threshold voltage, the mobility and transconductance degradation factor. The analytical predictions are in very close agreement with three-dimensional (3D) numerical simulations results in spite of the simplification used in the both operating regions.**

Keywords—Diamond layout style, Zero temperature coefficient, Simple model, Mobility degradation

I. INTRODUCTION

High temperature electronics is a large value market that has been difficult to serve up till now. In the automotive field, on-engine and on-transmission applications are projected to require maximum temperatures of up to 200 °C with the wheel-mounted applications going even higher. Further high-temperature application areas include aerospace and environmental monitoring, such as mining and well logging [1].

In MOSFETs, only the top region (0.1-0.2 mm thick) of the silicon wafer is useful for electron transport. Silicon-on-Insulator (SOI) technology is emerging as the most mature solution for high-temperature applications in the MOS technology area. Indeed, SOI MOSFETs present lower leakage currents than bulk devices at high temperature, as well as a smaller variation of threshold voltage with temperature [2]. They are also immune to temperature-induced latchup. As a result, SOI circuits can operate at temperatures above 300 °C, while bulk CMOS is usually limited to 150 °C [3].

The key to the design of high-temperature analogue CMOS ICs is biasing all circuit stages at ZTC drain currents, which requires that appropriate gate voltages V_{GF} at ZTC (V_{ZTC}) be available on chip. For a given CMOS process, the magnitude of V_{ZTC} is fixed for all n- and p-MOSFETs, and the desired value of the corresponding I_{DS} at ZTC (I_{ZTC}) is obtained by adjusting the W/L ratio [4].

The ZTC is a very important bias point for analog designers as it corresponds to a gate voltage at which the device DC performance remains constant with temperature [1], i.e., $dI_{DS}(T)/dT \sim 0$. This can be explained as follows. The ZTC gate bias point (V_{ZTC}) is the value of V_{GF} at which the reduction of the threshold voltage is counter-balanced by the reduction of the mobility, and as a result, the value of the drain current remains constant as the temperature varies. For gate voltages lower than V_{ZTC}, the decrease of threshold voltage is dominant and so the drain current increases with temperature, while for gate voltages higher than V_{ZTC}, the mobility degradation predominates and the drain current decreases with temperature.

It is expected that the mutual compensation of the mobility and the threshold voltage temperature dependences may result in a stable ZTC bias point for MOSFETs. However, the mobility compensation is sometimes not enough to satisfy stability in the ZTC point bias [5]. Also, it has been confirmed that ZTC point models should be as simple as possible in order to enable efficient circuit prediction.

Previous studies, based on three-dimensional (3D) numerical simulations and experimental data, have demonstrated the benefits of DSL at room T in terms of drain current (I_{DS}), transconductance (g_m), g_m/I_{DS}, on-state resistance (R_{ON}), on-state I_{DS} (I_{ON}), Early Voltage (V_{EA}), intrinsic voltage gain (A_V) and unit voltage gain frequency (f_T) [6–11]. The Diamond layout style for MOSFET is capable to keep active the LCE and PAMDLE effects under high temperature environment (300–573 K) and consequently remarkable improvements the analog and digital electrical performance of SOI MOSFETs, mainly regarding the saturation drain current and unit voltage gain frequency, practically without degrading the voltage gain [12].

The goal of this work is to study the ZTC bias point for the Diamond layout style devices based on three-dimensional (3D) numerical simulations data. A simple ZTC analytical model is also used, in order to validate this results.

II. THE DSM STRUCTURES AND THE DEVICES CHARACTERISTICS

The innovative MOSFETs structure Diamond SOI MOSFET (DSM)" [13] was created based on drain/silicon-film (channel region)/source interfaces engineering approach in order to offer a better alternative to the analog integrated circuits specific applications.

A modification of the gate geometric shape from rectangular (conventional) to hexagonal was performed (Fig. 1) in order to enhance the longitudinal electrical field ($\varepsilon_{//\_DSM}$), the average drift velocity of the mobile carriers in the channel (v_x), the drain current (I_{DS}), the transconductance (g_m) and to reduce the on-resistance (R_{DSon}), now by using the ''corner effect" along the channel longitudinal (parallel) direction named ''Longitudinal Corner Effect" (LCE), without any extra burden to the current technology.

Figure 1 illustrates the top views of the DSM (Fig. 1a) and its corresponding CSM counterpart (Fig. 1b), regarding the same A_G, where the b and B are the lengths of the two bases (minor and major) of two trapezoids that compose the hexagonal gate region of the DSM, respectively, the W is the channel width, the α is the angle between the metallurgical pn junctions of the source/silicon-film (channel region) and the silicon-film/drain regions, $\varepsilon_{//\_DSM}$ is the resultant longitudinal electric field (LEF) at the point P of the DSM, due the drain bias (V_{DS}), which is given by the vector sum of two LEF components, $\varepsilon_{//1}$ and $\varepsilon_{//2}$ (LCE effect) [7–11, 14], the L is the CSM channel length and the $\varepsilon_{//\_CSM}$ is the longitudinal electric field of the CSM. Considering the point P in these two transistors, we can observe that the $\varepsilon_{//\_DSM}$ is higher than the one found in the CSM counterpart ($\varepsilon_{//\_CSM}$), due to the LCE effect, regarding the same A_G and bias conditions.

In order to implement two SOI MOSFETs with similar gate areas (A_G), where one is implemented with the hexagonal gate shape (Diamond layout style) and the other is implemented with the standard (rectangular) gate geometry, it is necessary that the channel length (L) of the CSM is equal to (b + B)/2. However, the DSM can be electrically represented by the parallel association of infinites infinitesimal CSMs, with the same channel width and with different channel lengths (Li), where $b \leq L_i \leq B$ and i is an integer number ($0 \leq \leq \infty$). Regarding this approach, its effective channel length (Leff) can be obtained and it is calculated by (B-b)/ln(B/b) [11]. If we consider the same A_G of a DSM and a CSM counterpart, the DSM Leff is smaller than the CSM L [=(b + B)/2] and therefore the Diamond layout style for MOSFETs is capable to present a higher drain current (I_{DS}) than the one found in the equivalent CSM, regarding the same bias conditions. The dimensional characteristics of the DSM and their CSMs counterparts used to perform the experimental work are indicated in Table 1.

Table I. Dimensions of the devices used for this simulated work.

λ = 0.35μm						
Device	**A_G** [λ^2]	**W** [λ]	**L** [λ]	**B** [λ]	**b** [λ]	**α**
DM59	484.5	17	28.5	54.0	3.00	36.9°
DM41	340.0	17	20.0	37.0	3.00	53.1°
DM23	195.5	17	11.5	20.0	3.00	90.0°
DM14	119.0	17	7.25	11.5	3.00	126.9°
DM11	93.5	17	5.75	8.5	3.00	144.1°

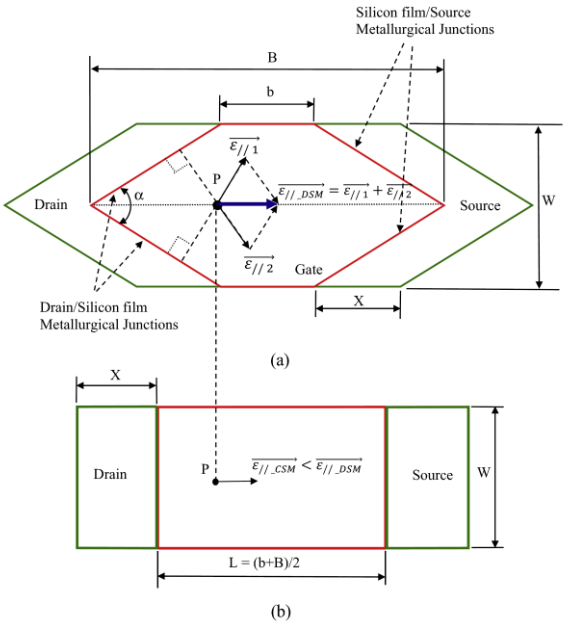

Fig. 1. The top schematic views of DSM (a) and its CSM counterpart (b), regarding the same gate area and its corresponding longitudinal electric field components.

III. ZTC ANALYTICAL MODEL

To evaluate the ZTC was analyzed using the CM (Camilo/Martino) ZTC analytical model [15], the V_{GF} value obtained by the cross point between the drain current I_{DS} versus the gate voltage V_{GF} curves for two temperatures T1 and *T2*, is defined as $V_{ZTC\ 1,2}$ as shown in conceptual figure 2.

Therefore, $V_{ZTC\ 1,2}$ can be calculated as shown in equations (1) for the linear and (2), (3) and (4) for the saturation region [15].

$$V_{ZTC\ 1,2\ (LIN)} = A + n\,V_{DS}/2 \quad (1)$$

$$V_{ZTC\ 1,2\ (SAT)} = A + (A^2 - B)^{1/2} \quad (2)$$

Where

$$A = (\mu_{n1}\,V_{th1} - \mu_{n2}\,V_{th2})/(\mu_{n1} - \mu_{n2}) \quad (3)$$

$$B = (\mu_{n1}\,V_{th1}{}^2 - \mu_{n2}\,V_{th2}{}^2)/(\mu_{n1} - \mu_{n2}) \quad (4)$$

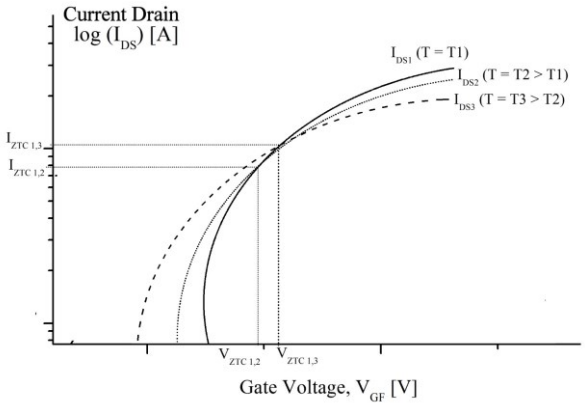

Fig. 2. The ZTC point between temperature *T1, T2* and *T3*..

and V_{th} is the threshold voltage, μn is the effective mobility, where the index 1 means that the parameters were obtained in the temperature reference T_1 = 300 K.

Considering that the mobility temperature degradation (and consequently the transconductance), can be modeled by equation (5), the body factor $n_1 \approx n_2 \approx n$ and the mobility degradation due to the transverse electric field $\theta_1 \approx \theta_2$, thus $V_{ZTC\ 1,2}$ can be calculated based on equations (6) for the linear and (2), (7) and (8) for the saturation region, respectively.

$$(g_{m1}/g_{m2}) = (\mu_{n1}/\mu_{n2}) = (T1/T2)^C \quad (5)$$

$$V_{ZTC\ 1,2} = A + n\,V_{DS}/2 \quad (6)$$

$$A = V_{th1} + \left((V_{th1} - V_{th2})(T1/T2)^C\right)/(1 - (T1/T2)^C) \quad (7)$$

$$B = \left(\left({V_{th1}}^2 - {V_{th2}}^2\right)(T1/T2)^C\right)/(1 - (T1/T2)^C) \quad (8)$$

where c is the temperature mobility (or transconductance degradation factor and can be calculated by equation (9).

$$c = \log(g_{m1}/g_{m2})/\log(T1/T2) \quad (9)$$

It is implicit in equation (9) that the conduction mechanism is taking place predominately at the front interface; otherwise gm would not be only proportional to mobility but also influenced by the conduction mechanism path.

IV. Simulation Results and Discussion

Simulations of the Diamond transistor type MOSFET (DSM) were performed by using the SILVACO TCAD tools. SILVACO TCAD tool called DevEdit3D was used to generate the device structure and ATLAS was used to simulate the current–voltage characteristics [16].

The devices with diamond gate geometry were implemented in Partially-Depleted (PD) SOI nMOSFETs, considering the gate area (A) and geometric factor (W/L), as indicated in Table 1, considering 2 nm for t_{ox}, 100 nm for t_{si} and 400 nm for t_{box}, and the channel and drain/source doping concentrations equal to 5.5 x 10^{17} cm^{-3} and 1 x 10^{20} cm^{-3}, respectively.

Figure 3 shows the drain current (I_{DS}) as a function of gate-source voltage (V_{GS}) with the temperature ranging from 300 to 500 K in the linear and saturation regions of the DMs structures with its respective ZTC point.

By definition, the ZTC point represents the gate bias which ensures that the drain current remains constant with temperature variations [17]. This point is reached when the temperature mobility reduction compensates the threshold voltage shift with T. The decrease of mobility and threshold voltage are the main contributing factors to the position of the ZTC point [18].

In both operating regions, by Eq. (6) and Eq. (2) shows that when the temperature increases, (V_{th1}-V_{th2}) increases and $[T1/T2]^c$ decreases. The competition of these two terms depends on the value of the c coefficient, which is responsible for the V_{ZTC} changes as a function of tempera-ture. The V_{th1} and V_{th2} used in Eqs. (6) and (2) are the values obtained by

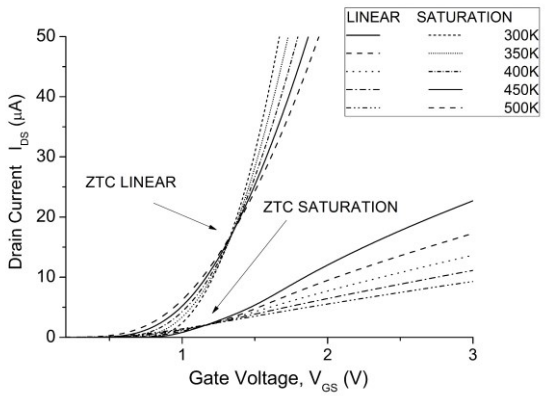

Fig. 3. I_{DS} x V_{GS} curves simulated obtained of the Diamond transistor type MOSFET (DM) devices for a temperature range from 300 up to 500 K in linear (V_{DS} = 50mV) and saturation region (V_{DS} = 1.5V).

simulations for each temperature, using the double derivative method[19].

To determine the best c values to fit the simulated data a simple arithmetic mean of the values obtained in each interaction between the different simulated temperatures, for both operating regime linear and saturation.

Fig. 4 show the V_{ZTC} values, obtained by simulations and the simple model, in function of temperature for DM structure operating in linear and saturation regime.

A reasonable close agreement with simulated results is observed even though some simplifications were adopted

V. Conclusions

In this work a simple model to determine the ZTC point was used to investigate MOSFET in Diamond (DM) gate geometry, considering over the temperature range from 300 up to 500 K in both linear and saturation regions..

In order to validate the model simulation results were used and presented good agreement. The maximum error found is

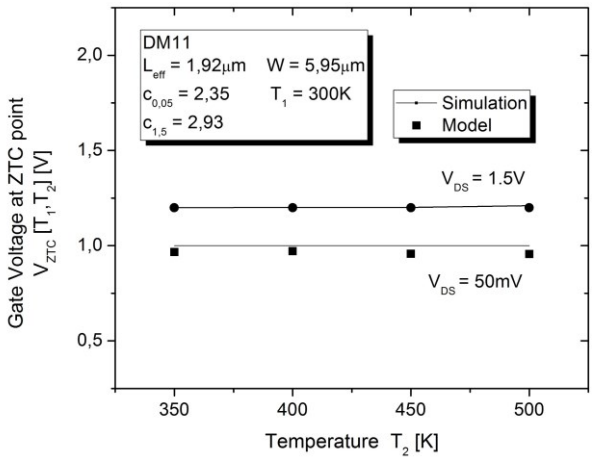

Fig. 4. V_{ZTC} obtained by simulations and the simple model for DM11 device (A_G = 11,45 [μm^2]) operating in the linear and the saturation region.

11.40 % in the linear region and 9.53 % in the saturation region.

The simulated results for DM devices were compared with the data model and the best c values to fit the simulated data are close to 2.6 for linear region and are in the range from 1.5 up to 2.9 for saturation region.

In both the cases, comparing results obtained by the simple model with simulation data, a good agreement is found in spite of the simplification used in the model.

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